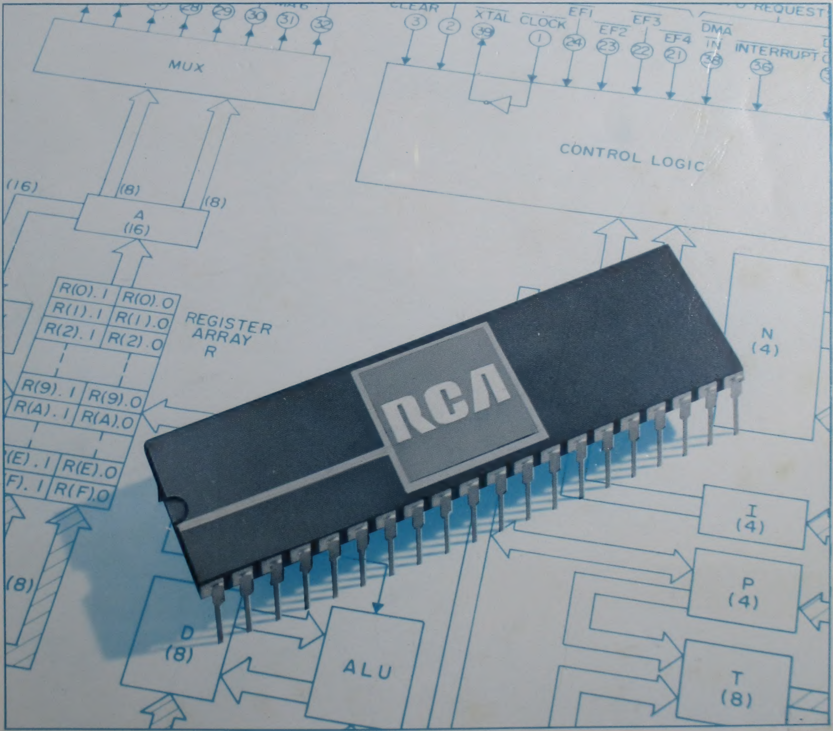
RCA Solid State

COSMAC Microprocessor Product Guide



MPG-180A

The RCA1800 microprocessor family includes all the elements you need to build an efficient microprocessor system.

Integrated Circuits (CDP1800 Series)

Our IC family boasts two important features: First, it's an all-CMOS family designed and manufactured by the First Family in CMOS. You get all the advantages of a CMOS system . . .

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- completely static circuitry
- wide temperature range (-55 to +125°C)
- high noise immunity
- CMOS, TTL, NMOS compatibility . . .

plus the CMOS production expertise only RCA can offer.

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- RAMs
- ROMs
- Input/Output (I/Os)
- System expanders

Support Systems (CDP18S Series)

RCA's theme in developing its hardware and software has been "Graduated Steps to Microprocessing". In both functions and dollar investment, we offer discrete, logical steps for you to follow. Our approach is to help you progress from a learning state right on through to integral hardware/software system prototyping, covering each step with an appropriate tool . . .

- COSMAC Microtutor II
- COSMAC Evaluation Kit
- COSMAC Microterminal
- COSMAC Development System II
- COSMAC Micromonitor
- Floppy Disk System
- Software Development Packages

All along the way, you'll use our manuals, application notes, and seminars to continually update your understanding of COSMAC.

CMOS technology, COSMAC architecture, and COSMAC support systems offer efficient, intelligent, economical programming and system design.

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The CDP1802 microprocessor is an 8-bit silicon-gate CMOS device for use as a general-purpose computing or control element.

Features:

- 8-bit parallel bidirectional data bus
- 16-x-16-bit matrix of registers for easy programming
- DC to 6.4-MHz clock (single phase)
- Fast 2.5- or 3.75-μs instruction time
- 91 basic instructions, 255 operation codes
- Minimal power-supply requirements – low current drain, single-supply, wide voltage range
- Split-power-supply option that allows for 10 V on internal parts of CPU and 5 V on interfacing lines
- Optional on-chip crystal-controlled oscillator
- Memory addressing to 65K bytes
- Adaptability to any combination of standard RAM, ROM, or PROM memories
- Maskable interrupt and 4 testable external flag lines
- On-chip DMA controls
- Simple RESET, $\overline{\text{LOAD}}$, PAUSE, and RUN controls
- Programmable serial output (Q)

CDP1800 Series ICs are available in two performance selections:

A type without a "C" suffix is the high-performance device. For example, the CDP1802 has:
- 4 V to 12 V recommended operating voltage range
- 2.5- or 3.75-μs instruction time
- 100-mW power dissipation (typical)
- 6.4-MHz maximum clock input frequency at 10 V.

A type with a "C" suffix, for example, the CDP1802C has:
- 4 V to 6 V recommended operating voltage range
- 5- or 7.5-μs instruction time
- 10-mW power dissipation (typical)
- 3.2-MHz maximum clock input frequency at 5 V

The Unique COSMAC Architecture

The COSMAC architecture is shown at the top of the facing page. The principal feature of this system is a register matrix consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated or selected by the 4-bit binary code from one of the designators P, X, or N. The contents of any register can be directed to any one of the following three paths:

1. to the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. to the accumulator (either of the two bytes can be gated to it);
3. to the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

How It Works

The registers in R can be used by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters – Any register can be used as the main program counter; the number of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction, the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the interrupt servicing routine, and at startup R(O) is the program counter. At other times, the register designated as program counter is at the discretion of the user.

Data Pointers – The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see the Instruction Summary on pages 28–29):

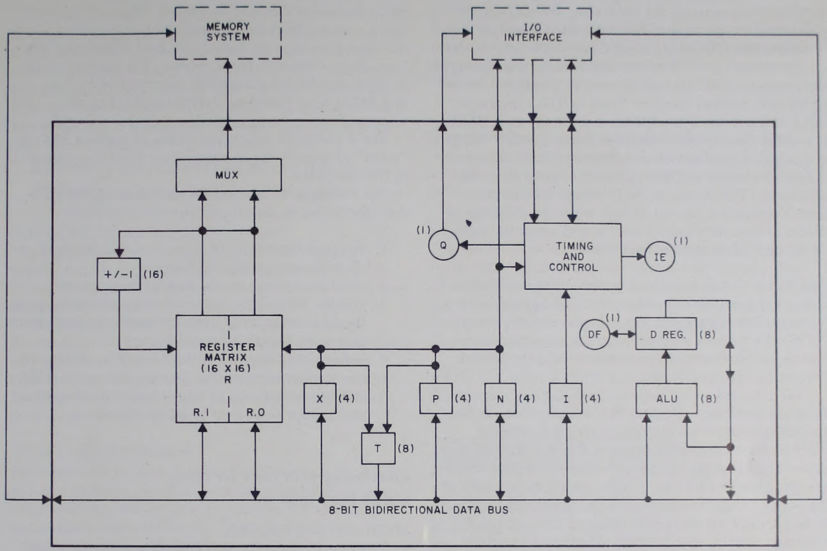
1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions (F8-FD, FF, 7C, 7D, 7F). During these instruction executions, the operation is referred to as "data immediate."

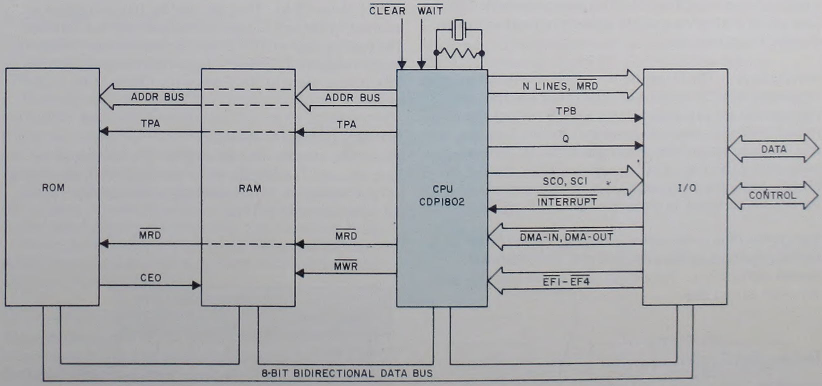
When interrupts are being serviced, register R(2) is used as the data (stack) pointer for the interrupt servicing routine. Similarly, register R(0) is the DMA pointer when Direct Memory Access is used.

Data Registers – When registers in R are used to store bytes of data, four instructions are provided (8N, 9N, AN, BN) which allow D to receive from or write into either the lower-order or higher-order byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

CDP1802 COSMAC architecture



Typical CDP1802-based microcomputer system



DMA —Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-in or DMA-out request is received, the current instruction cycle is completed before the request is serviced. Upon entering the DMA state, the contents of R(O) is sent to memory to determine the address the data is written into (DMA-in) or read from (DMA-out). At the completion of each DMA cycle, which is one machine cycle, the contents of R(O) is incremented by 1 so that it points to the next memory location. Thus, R(O) is a dedicated DMA data pointer; if the DMA feature is not used, R(O) is available for any other function. (Since the CDP 1802 is a static machine and no refreshing is needed, there is no maximum number of DMA cycles that can be done consecutively.) This feature in the COSMAC architecture saves a substantial amount of logic when fast exchange of blocks of data are required, such as with magnetic disks or during CRT-display-refresh cycles.

Load Mode — A program load facility, using the DMA-in channel, is provided to enable users to load programs into memory. This facility provides a simple, one-step means for initially entering programs into the microprocessor system and eliminates the requirement for a specialized "bootstrap" program loader.

Interrupt Servicing — Register R(1) is always used as the program counter when interrupt servicing is initiated. When an interrupt request comes in and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction) the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values: 2 in X and 1 in P. Interrupt enable is automatically deactivated to inhibit further interruptions. The user written interrupt routine is now in control. The contents of T can be saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the return routine restores the pre-interrupted values of X and P with a single instruction (70 or 71). The interrupt-enable flip-flop can be enabled to permit further interrupts or can be disabled to prevent them.

Accumulator — The D register is an 8-bit accumulator. Connected directly to the ALU, the D register provides one operand for any arithmetic or logic function. The second operand is found in memory. Results from the ALU's operation are then stored back into D, appropriately setting the 1-bit data flag register (DF). A series of branch, shift, and arithmetical instructions are provided for operations based on either the value of D or DF.

The Q Flip-Flop — An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a bit serial output line.

Instruction Cycles

COSMAC instructions consist of two machine cycles, a fetch cycle and an execute cycle (except for CN instructions, which require two execute cycles). Each machine cycle is 8 clock pulses long. During the fetch cycle, the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by 1 so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. select an input or output port for data transfer;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, etc.,
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

Conversing with the CDP1802: Signal Descriptions

BUS 0 to BUS 7 (Data Bus)
8-bit bidirectional DATA BUS lines. These lines are used for transferring data among the memory, the microprocessor, and the I/O devices.

TPA, TPB (2 Timing Pulses)
Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

SC0, SC1 (2 State Code Lines)
These lines indicate that the CPU is: (1) fetching an instruction, or (2) executing an instruction, or (3) processing a DMA request, or (4) acknowledging an interrupt request. All states are valid at TPA.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

HIGH = V_{CC}
LOW = V_{SS}

$\overline{\text{MWR}}$ (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{\text{MRD}}$ (Read Level)

A low level (V_{SS}) on $\overline{\text{MRD}}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, $\overline{\text{MRD}}$ is useful for driving memory bus separators. It is also used to indicate the direction of data transfer during an I/O instruction:

$\overline{\text{MRD}}=V_{CC}$: Data from I/O to CPU and Memory

$\overline{\text{MRD}}=V_{SS}$: Data from Memory to I/O or CPU

MA0 to MA7 (8 Memory Address Lines)

The higher-order byte of a 16-bit COSMAC memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system are strobed into external address latches by timing pulse TPA. (The CDP1831 and CDP1833 ROM's have built-in-address latches as well as other system-simplifying features, as listed on page 11.) The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 65K bytes.

N0, N1, N2 (I/O Selection)

These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding three lower order bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 and is indicated by the level of the $\overline{\text{MRD}}$ signal.

$\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$ (3 I/O Requests)

These inputs are sampled by the CDP1802 during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit) requiring one machine cycle; and instruction execution is resumed by fetching the next instruction from M(R(1)).

DMA Action: Finish executing current instruction; R(O) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(O).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority, followed by DMA-OUT and then INTERRUPT.

$\overline{\text{EF1}}$ to $\overline{\text{EF4}}$ (4 Flags)

These inputs enable the I/O controllers to transfer status information to the processor. The lines can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flags. The flags are sampled at the beginning of every S1 cycle.

Q Flip-Flop

Single-bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK

Input for externally generated single-phase clock. The maximum clock frequency is 6.4 MHz at $V_{CC} = V_{DD} =$ 10 volts. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{\text{XTAL}}$

Connection to be used with clock input terminal for an external crystal if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{\text{XTAL}}$) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be used for precise frequency adjustments.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ (2 Control Lines)

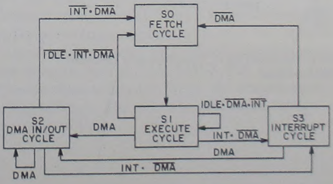
Provide four control modes as listed in the following truth table:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
H	H	RUN
H	L	PAUSE
L	H	RESET
L	L	LOAD

The functions of the modes are defined as follows:

Run – May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

The CDP1802 state transitions when in the RUN mode are shown below. Each machine cycle requires the same period of time – 8 clock pulses. The execution of an instruction pulse requires either two or three machine cycle, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response.

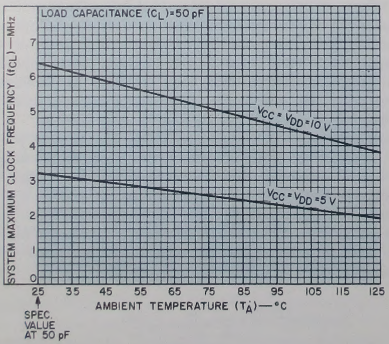

$\overline{\text{INT}}\cdot\overline{\text{DMA}}$
S0
FETCH
CYCLE
$\overline{\text{DMA}}$
$\overline{\text{IDLE}}\cdot\overline{\text{INT}}\cdot\overline{\text{DMA}}$
IDLE$\cdot\overline{\text{DMA}}\cdot\overline{\text{INT}}$
S2
DMA IN/OUT
CYCLE
DMA
S1
EXECUTE
CYCLE
INT$\cdot\overline{\text{DMA}}$
S3
INTERRUPT
CYCLE
DMA
INT$\cdot\overline{\text{DMA}}$
DMA

RECOMMENDED OPERATING CONDITIONS

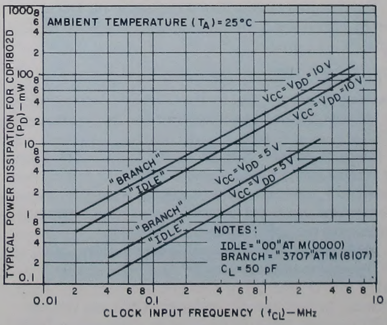
CHARACTERISTIC	CONDITIONS		LIMITS AT 25°C		UNITS
	V_{CC}[1] (V)	V_{DD} (V)	CDP1802D	CDP1802CD	
Supply-Voltage Range	–	–	4 to 12	4 to 6	V
Input Voltage Range	–	–	V_{SS} to V_{CC}	V_{SS} to V_{CC}	V
Maximum Clock Input Rise or Fall Time, t_r or t_f	4–12	4–12	1	1	µs
Instruction Time[2]	5	5	5	5	µs
	5	10	4	–	
	10	10	2.5	–	
Maximum DMA Transfer Rate	5	5	400	400	KBytes/sec
	5	10	500	–	
	10	10	800	–	
Maximum Clock Input Frequency, f_{CL}[3]	5	5	DC – 3.2	DC – 3.2	MHz
	5	10	DC – 4	–	
	10	10	DC – 6.4	–	

NOTES:

1. $V_{CC} \leqslant V_{DD}$; for CDP1802CD $V_{CC} = V_{DD} = 5$ volts.
2. Equals 2 machine cycles–one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles–one Fetch and two Execute operations.
3. Load Capacitance (C_L) = 50 pF.



Typical maximum clock frequency as a function of temperature.



Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction for CDP1802D.

ELECTRICAL CHARACTERISTICS

Static

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
				VALUES				+25			
	V_O (V)	V_{IN} (V)	V_{CC}, V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_L Max.	–	–	5	–	–	–	–	–	1	100	µA
	–	–	10	–	–	–	–	–	10	500	
CDP1802D	–	–	15	–	–	–	–	–	–	1000	
CDP1802CD	–	–	5	–	–	–	–	–	–	500	
Output Low Drive (Sink) Current, I_{OL} Min. (Except $\overline{XTAL}$)	0.4	0,5	5	1.98	1.89	1.14	0.90	1.5	2.2	–	mA
	0.5	0,10	10	3.70	3.53	2.13	1.68	2.8	5.2	–	
$\overline{XTAL}$ Output I_{OL} Min.	0.4	5	5	132	126	76	60	100	–	–	µA
Output High Drive (Source Current) I_{OH} Min. (Except $\overline{XTAL}$)	4.6	0,5	5	–0.46	–0.44	–0.27	–0.21	–0.35	–0.51	–	mA
	9.5	0,10	10	–1.12	–1.07	–0.65	–0.51	–0.85	–1.3	–	
$\overline{XTAL}$ Output I_{OH} Min.	4.6	0	5	66	63	38	30	–50	–	–	µA
Output Voltage Low-Level V_{OL} Max.	–	0,5	5	0.00				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
Output Voltage High Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	0.5,4.5	–	5,10	1				–	–	1	
	1,9	–	10	3				–	–	3	
Input High Voltage V_{IL} Max.	0.5,4.5	–	5	3.5				3.5	–	–	
	0.5,4.5	–	5,10	4				4	–	–	
	1,9	–	10	7				7	–	–	

Pause – Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

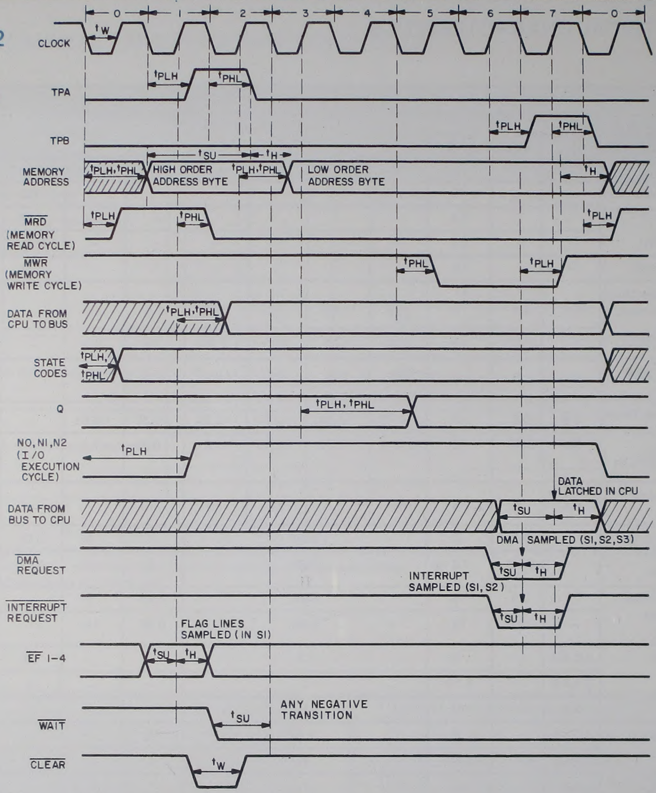
Reset – Registers I, N, Q are reset, IE is set, and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle. During this cycle the CPU remains in S1 and registers X, P, and R(O) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or S2. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE so as to preclude interrupts until ready for them. Power-up reset can be realized by connecting a buffered RC network to $\overline{\text{CLEAR}}$.

Load – Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that the termination of the DMA-in operation does not force execution of the next instruction.

V_{DD}, V_{SS}, V_{CC} (Power Levels)

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at high speed while interfacing with lower voltage elements such as TTL, NMOS, and LEDs. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.

CDP1802 Timing Diagram



NOTES:

1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE
2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS
3. SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD

CDP1802 INSTRUCTION EXECUTION TIMES

1-Byte instructions require 2 Machine Cycles: 1 Fetch, 1 Execute.

2-Byte instructions also require 2 Machine Cycles: 1 Fetch, 1 Execute.

3-Byte instructions require 3 Machine Cycles: 1 Fetch, 2 Executes.

INSTRUCTION SIZE			% OF TOTAL REPERTOIRE	INSTRUCTION TIME @ f =		
Bytes of Op. Code	Bytes of Address or Data	Total Bytes of Memory		6.4 MHz	3.2 MHz	2 MHz
1	0	1	93	2.5 µs	5 µs	8 µs
1	1	2				
1	2	3	7	3.75 µs	7.5 µs	12.1 µs
Average Instruction Execution Time			–	2.6 µs	5.2 µs	8.3 µs

Memory System Circuits for the CDP1802 include CMOS ROMs and RAMs with many system-simplifying capabilities

Features:

- Low power consumption
- All fully static parts
- Single power supply
- Direct interfacing with 1800-series microprocessor systems
- 3-state outputs
- TTL drive capability
- Industry standard pin-outs
- Different parts designed for small, medium, or large memory systems

Parts List:

ROMs (custom)

512 X 8	CDP1831
512 X 8	CDP1832
1024 X 8	CDP1833
1024 X 8	CDP1834

ROMs (standard)

Utility Program UT4	CDPR512
Microterminal Controller UT5	CDPR522

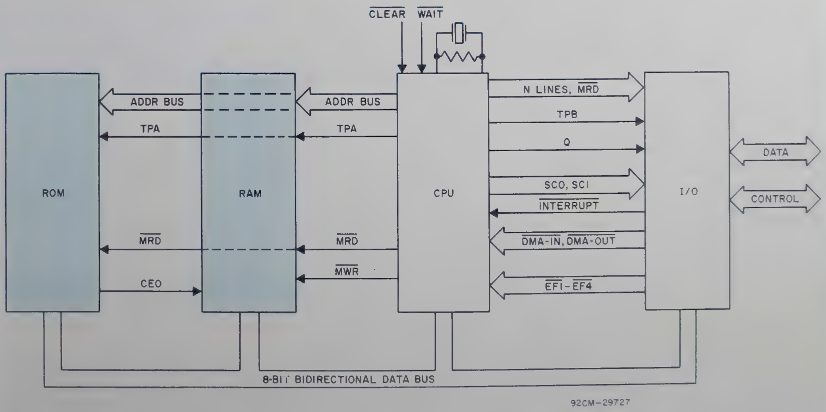
RAMs

1024 X 1	CDP1821S
256 X 1	CDP1822S
128 X 8	CDP1823S
32 X 8	CDP1824

System Expanders

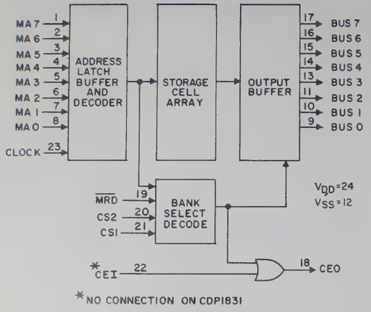
4-Bit Bus Buffer/ Separator	CDP1856
Memory Address Latch with Dual 1 of 4 Decoders	CDP1858
Memory Address Latch with 1 of 4 Decoder	CDP1859

Typical CDP1802-based microcomputer system



512x8 ROM CDP1831

1024x8 ROM CDP1833

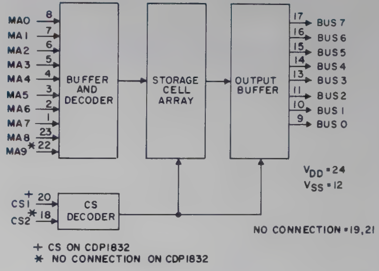


*NO CONNECTION ON CDP1831

- User programs ROM's location in memory field
- Mask programmable
- On-chip latch for higher-order memory address
- CEO signal indicates status of chip (selected or not)
- Can minimize or eliminate memory decoding logic
- Either 512 or 1024 bytes of ROM in same pin-out
- 3 chip selects
- 3-state outputs
- Single power supply
- Industry standard 24-pin packages
- 400-ns access time at 10 V
- Directly compatible with CDP1802

512x8 ROM CDP1832

1024x8 ROM CDP1834



+ CS ON CDP1832
* NO CONNECTION ON CDP1832

- CDP1832 is pin compatible with the 2704 PROM
- CDP1834 is pin compatible with the 2708 PROM
- Directly compatible with the CDP1802
- Mask programmable
- Single power supply 400-ns access time at 10 V
- 3-state outputs
- Industry standard 24-pin packages
- Accepts standard memory address decoding

Standard Program ROMs

Utility Program UT4 CDPR512

Mask-programmed CDP1832 512 x 8 ROM for use in the COSMAC Evaluation Kit (CDP18S020).
Includes routines for:
- ASCII-code conversion
- Memory read and write commands
- System initialization

Microterminal Controller UT5 CDPR522

Mask-programmed CDP1832 512 x 8 ROM for use with the COSMAC Microterminal (CDP18S021).
Includes routines for:
- Keyboard scan and debounce
- Digit, segment, and decimal point controls for a display
- Memory read and write commands

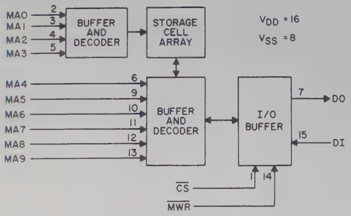
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	Non-"C" Types		"C" Types		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range	–	4	12	4	6	V
Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS

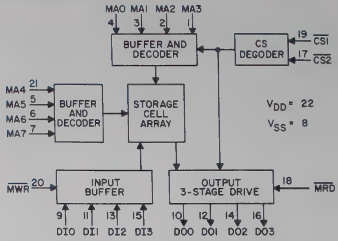
CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES AT $T_A = 25^\circ C$								UNITS
	V_O (V)	V_{DD} (V)	CDP-1831D	CDP-1831CD	CDP-1832D	CDP-1832CD	CDP-1833D	CDP-1833CD	CDP-1834D	CDP-1834CD	
Static											
Quiescent Device Current, I_L Max.	–	5	100	1000	100	1000	100	1000	100	1000	µA
	–	10	500	–	500	–	500	–	500	–	
	–	15	1000	–	1000	–	1000	–	1000	–	
Output Low Drive (Sink) Current, I_{OL} Min.	0.4	5	0.8	0.8	0.8	0.8	3.2	3.2	3.2	3.2	mA
	0.5	10	1.8	–	1.8	–	7.2	–	7.2	–	
Output High Drive (Source) Current, I_{OH} Min.	4.6	5	–0.8	–0.8	–0.8	–0.8	–2	–2	–2	–3.2	
	9.5	10	–1.8	–	–1.8	–	–5	–	–5	–	
Dynamic: $t_r, t_f = 10$ ns, $C_L = 50$ pF											
Access Time From Address Change, t_{AA}	–	5	850	850	850	850	850	850	850	850	ns
	–	10	400	–	400	–	350	–	350	–	
Access Time From Chip Select, t_{ACS}	–	5	–	–	400	400	700	700	700	700	ns
	–	10	–	–	200	–	300	–	300	–	
Chip Enable Output Delay Time From CS, t_{CO}	–	5	400	400	–	–	400	400	–	–	ns
	–	10	200	–	–	–	200	–	–	–	

1024x1 RAM
CDP1821S



- Interfaces with CDP1802 at full speed
- Good for large RAM memory systems
- Single power supply
- Industry standard 16-pin packages for high board density
- 200-ns access time at 10 V
- CS can be used as an additional address line — no clocking required
- Standby power consumption of 5 mW (typ.) at 10 V

256x4 RAM
CDP1822S



- Interfaces with CDP1802 at full speed
- 2 chip selects for easy memory expansion
- 200-ns access time at 10 V
- Output disable permits common I/O systems
- Industry standard 22-pin packages
- Standby power consumption of 5 mW (typ.) at 10 V

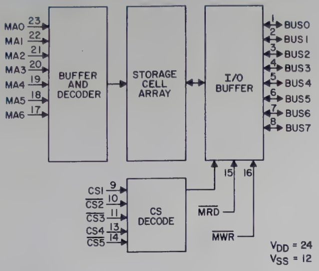
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	Non-"C" Types		"C" Types		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range	—	4	10	4	6	V
Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS

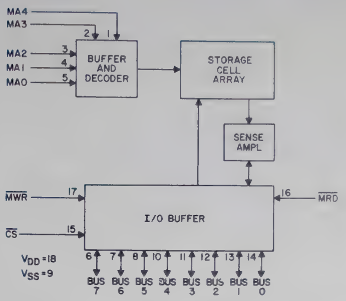
CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES AT $T_A = 25°C$				UNITS
		V_O (V)	V_{DD} (V)	CDP-1821SD	CDP-1821SDC	CDP-1822SD	CDP-1822SCD	
Static								
Quiescent Device Current, I_L Max.		— —	5 10	300 1500	1500 —	300 1500	1500 —	μA
Output Low Drive (Sink) Current I_{OL} Min.	Any Output	0.4 0.5	5 10	2.5 3.5	2.5 —	.4 1.8	.4 —	mA
Output High Drive (Source) Current I_{OH} Min.	Any Output	4.6 9.5	5 10	−1.25 −1.5	−1.25 —	.4 −1.8	.4 —	
Dynamic: t_r, t_f = 10 ns, C_L = 50 pF								
Read Operation								
Access Time From Address Change, t_{AA}		— —	5 10	350 200	350 —	350 200	350 —	ns
Access Time From Chip Select, t_{AC}		— —	5 10	260 160	260 —	260 160	260 —	ns
Total Power-Dissipation, P_D at 1 μs cycle		— —	5 10	5 20	8 —	8 35	10 —	mW

128x8 RAM
CDP1823S



- 3-state bus
- Directly interfaces with CDP1802
- Standby power consumption of 5 mW (typ.) at 10 V
- Single power supply
- 200-ns access time at 10 V
- Industry standard 24-pin packages
- Designed for medium-sized RAM requirements

32x8 RAM
CDP1824



- 300-ns access time at 10 V
- Fully decoded and static
- Separate read and write signals
- Standby power consumption of 5 mW (typ.) at 10 V
- Low quiescent and operating power
- Excellent for minimum RAM systems (e.g., stacks)
- Industry standard 18-pin packages
- $\overline{CS}$ for memory expansion

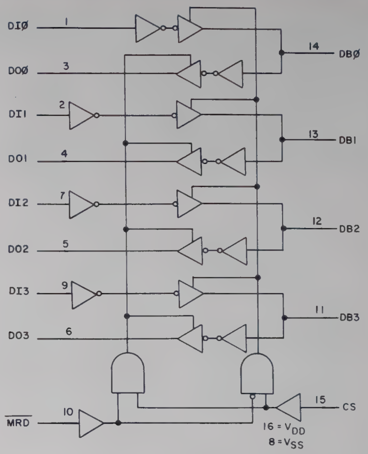
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	Non-"C" Types		"C" Types		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range	–	4	10 (CDP1823S) 12 (CDP1824)	4	6	V
Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES AT $T_A = 25°C$				UNITS
		V_O (V)	V_{DD} (V)	CDP-1823SD	CDP-1823SCD	CDP-1824D	CDP-1824CD	
Static								
Quiescent Device Current, I_L Max.		– –	5 10	300 1000	1500 –	100 500	500 –	µA
Output Low Drive (Sink) Current I_{OL} Min.	Any Output	0.4 0.5	5 10	1.2 1.8	1.2 –	2.2 4 2	2.2 –	mA
Output High Drive (Source) Current I_{OH} Min.	Any Output	4.6 9.5	5 10	–0.8 –1.8	–0.8 –	–1.1 7.2	–1.1 –	
Dynamic: t_r, $t_f = 10$ ns, $C_L = 50$ pF								
Read Operation								
Access Time From Address Change, t_{AA}		– –	5 10	350 200	350 –	600 300	600 300	ns
Access Time From Chip Select, t_{AC}		– –	5 10	250 150	250 –	600 300	600 –	ns
Total Power-Dissipation, P_D at 1 µs cycle		– –	5 10	15 65	20 –	10 50	12 –	mW

4-Bit Bus Buffer/Separator
CDP1856 (Memory)



- Allows simple expansion of memory
- Connects directly to CPU's bidirectional data bus
- Non-inverting fully buffered data transfer
- Compatible with CDP1802 microprocessor at maximum speed
- CHIP SELECT input for simple system configurations
- Low quiescent and operating power

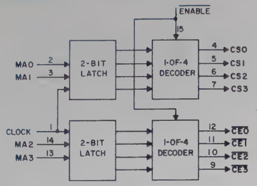
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1856D		CDP1856CD		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	—	4	12	4	6	V
Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS

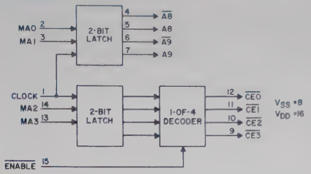
CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES AT T_A = 25°C		UNITS
		V_O (V)	V_{DD} (V)	CDP-1856D	CDP-1856CD	
Static						
Quiescent Device Current, I_L Max.		— — —	5 10 15	50 100 500	100 — —	μA
Output Low (Sink) Current, I_{OL} Min.	Any Output	0.4 0.5	5 10	1.6 3.6	1.6 —	mA
Output High (Source) Current, I_{OH} Min.	Any Output	4.6 9.5	5 10	−1.6 −3.6	−1.6 —	
Dynamic: t_r, t_f = 10 ns, C_L = 100 pF						
Propagation Delay Time: $\overline{\text{MRD}}$ or CS to DO, t_{ED}		— —	5 10	150 75	150 —	ns
$\overline{\text{MRD}}$ or CS to DB, t_{EB}		— —	5 10	150 75	150 —	ns
DI to DB, t_{IB}		— —	5 10	100 50	100 —	ns
DB to DO, t_{BD}		— —	5 10	100 50	100 —	ns

4-Bit Latch with Dual 1 of 4 Decoders
CDP1858



- For use with 256 x 4 (CDP1822) memories
- Low-power CMOS
- Fully static circuitry
- Enable pin for easy expansion above 4K byte memory systems
- Directly interfaces with CDP1802 microprocessor

4-Bit Latch with 1 of 4 Decoder
CDP1859



- Designed for use with 1024 x 1 (CDP1821) organized memories
- Low power usage
- Fully static circuitry
- Single 4-12V power supply
- Enable pin allows for easy expansion above 4K bytes of memory
- Directly interfaces with CDP1802 microprocessor

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1858D CDP1859D		CDP1858CD CDP1859CD		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range	–	4	12	4	6	V
Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			TYPICAL VALUES AT T_A = 25°C				UNITS
		V_O (V)	V_{DD} (V)	CDP-1858D	CDP-1858CD	CDP-1859D	CDP-1859CD	
Static								
Quiescent Device Current, I_L Max.		– – –	5 10 15	50 100 500	100 – –	50 100 500	100 – –	µA
Output Low (Sink) Current, I_{OL} Min.		0.4 0.5	5 10	1.6 3.6	1.6 –	1.6 3.6	1.6 –	mA
Output High (Source) Current, I_{OH} Min.		4.6 9.5	5 10	–1.6 –3.6	–1.6 –	–1.6 –3.6	–1.6 –	
Dynamic: t_r, t_f=10 ns, I_L=100 pF								
Propagation Delay Time: Clock_{LH} to CS0, CS1, CS2, or CS3	Enable=0	– –	5 10	220 110	220 –	– –	– –	ns
Clock_{LH} to A8, A9, $\overline{\text{A8}}$ or $\overline{\text{A9}}$		– –	5 10	– –	– –	200 100	200 –	ns
MA0, MA1 to CS0, CS1, CS2, or CS3	Clock=1 $\overline{\text{Enable}}$=0	– –	5 10	200 90	200 –	– –	– –	ns
MA2, MA3 to $\overline{\text{CE0}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, or $\overline{\text{CE3}}$	Clock=1 Enable=0	– –	5 10	200 90	200 –	– –	– –	ns
MA0, MA1 to A8; A9, $\overline{\text{A8}}$ or $\overline{\text{A9}}$	Clock=X	– –	5 10	– –	– –	150 75	150 –	ns
MA2, MA3 to $\overline{\text{CE0}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, or $\overline{\text{CE3}}$	Clock=1 $\overline{\text{Enable}}$=0	– –	5 10	– –	– –	200 90	200 –	ns

X = DON'T CARE

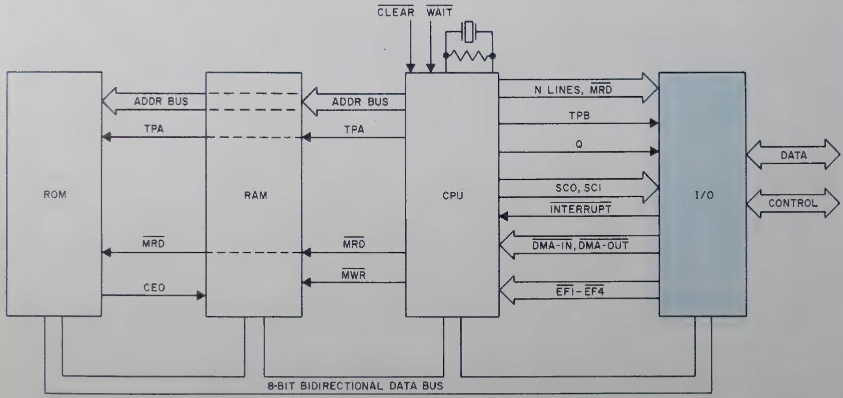
Input/Output System Circuits make use of many CDP1802 signals to lower cost and optimize performance.

Features:
- 4 CPU-tested flag inputs (EF lines) for binary inputs or for I/O-to-CPU signalling
- Interrupt request; maskable for flexibility
- 2 DMA request lines, in and out, with memory pointer and control logic on the CDP1802
- 2 state-code output lines to tell I/O devices what the CPU is doing
- Programmable output bit Q
- 3 I/O command lines (N) for programmed control of memory-I/O transfer
- Memory data strobe (TPB) for clean and easy capture of data by I/O device

Parts List:

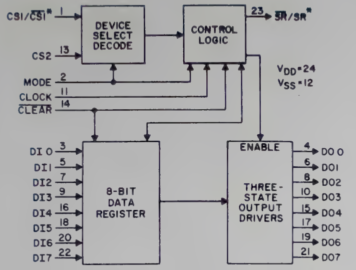
Byte I/O Port	CDP1852
N-Bit Decoder	CDP1853
UART (Universal Asynchronous Receiver/Transmitter)	CDP1854
4-Bit Bus Buffer/Separator (I/O)	CDP1857
Video Display Controller	CDP1861

Typical CDP1802-based microcomputer system



8-Bit Byte I/O Port

CDP1852

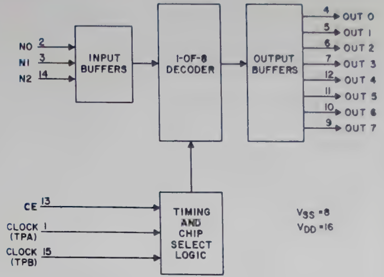


* POLARITY DEPENDS ON MODE

- 8-bit data latch
- Directly interfaces with CDP1802
- Industry standard 24-pin packages
- 3-state outputs
- Clear input
- Designed for use in 8-bit microprocessor systems
- Fully static
- Mode selectable

N-Bit Decoder

CDP1853



- Allows easy expansion of I/O systems
- Buffered inputs and outputs
- Functions at full microprocessor speed
- Ties directly to "N" lines on CDP1802
- Strobed outputs for spike-free decoding
- Low power dissipation
- Provides control of up to 14 I/O devices

RECOMMENDED OPERATING CONDITIONS

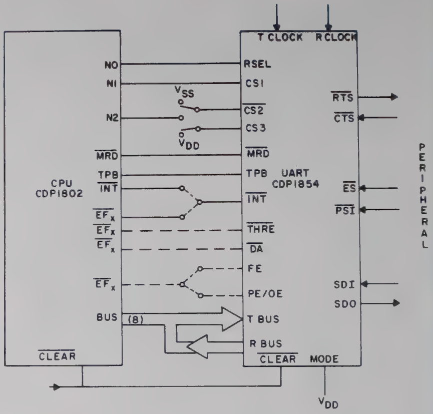
CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	Non-"C" Types		"C" Types		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range	–	4	12	4	6	V
Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES AT T_A = 25°C					UNITS
		V_O (V)	V_{DD} (V)	CDP-1852D	CDP-1852CD	CDP-1853D	CDP-1853CD	
Static								
Quiescent Device Current, I_L Max.		– – –	5 10 15	50 100 500	100 – –	50 100 500	100 – –	µA
Output Low (Sink) Current, I_{OL} Min.	Any Output	0.4 0.5	5 10	1.6 3.6	1.6 –	1.6 3.6	1.6 –	mA
Output High (Source) Current, I_{OH} Min.	Any Output	4.6 9.5	5 10	−1.6 −3.6	−1.6 –	−1.6 −3.6	−1.6 –	
Dynamic: t_r, t_f = 10 ns, C_L = 100 pF								
Propagation Delay Time: Output from CS, t_{CA}		– –	5 10	200 100	200 –	– –	– –	ns
Data to Output, t_{OD}		– –	5 10	200 100	200 –	– –	– –	ns
CE to Output, t_{EOH}, t_{EOL}		– –	5 10	– –	– –	200 100	200 –	ns
N to Outputs, t_{NOH}, t_{NOL}		– –	5 10	– –	– –	250 120	120 –	ns

UART
CDP1854

- Pin-out selectable by a single mode signal
- Mode O is pin-compatible with industry types 1602, 6011, etc.
- Mode 1 directly interfaces with 8-bit microprocessor like the CDP1802
- Single power supply
- False-start bit detection
- DC to 400K baud at 10 V
- Fully programmable with selectable:
  - parity inhibit
  - even/odd parity
  - 1, 1½, or 2 stop bits
- Overrun error detection
- External word length selection–5, 6, 7, or 8 bits
- Full or half duplex operation
- Full temperature range operation
- Low power dissipation–5 mW typ. at 5 V
- Standard 40-pin packages



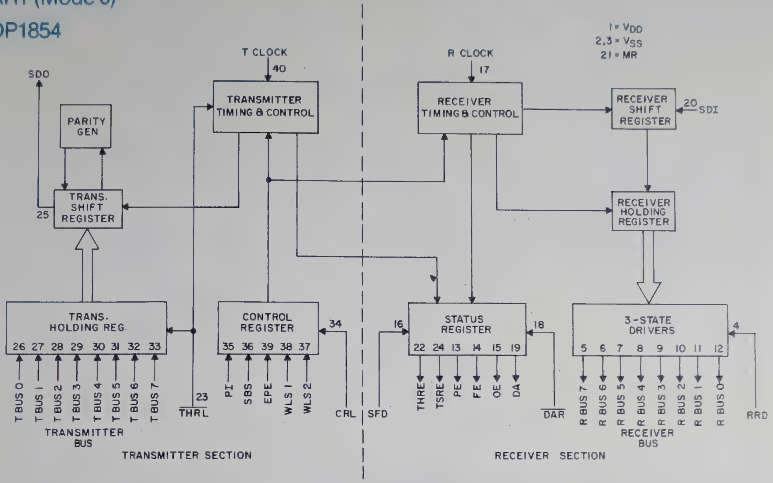
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1854D		CDP1854CD		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range	–	4	12	4	6	V
Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

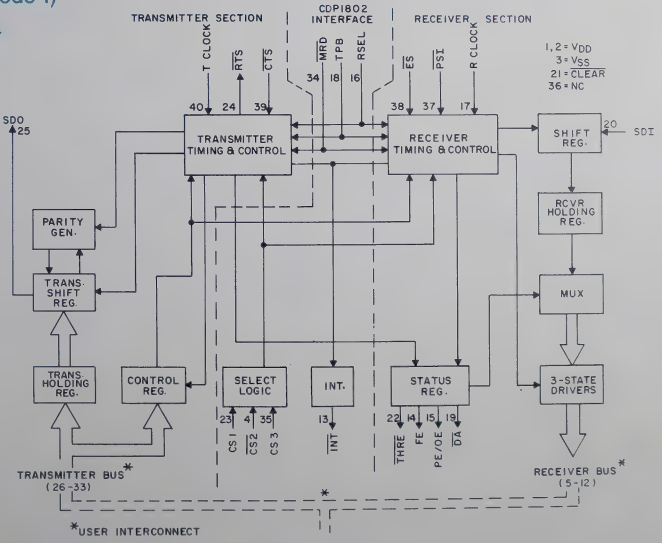
ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES AT $T_A = 25^\circ C$		UNITS
	V_O (V)	V_{DD} (V)	CDP1854D	CDP1854CD	
Static					
Quiescent Device Current, I_L Max.	–	5	100	500	µA
	–	10	500	–	
	–	15	1000	–	
Output Low (Sink) Current, I_{OL} Min.	0.4	5	0.4	0.4	mA
	0.5	10	0.9	–	
Output High (Source) Current, I_{OH} Min.	2.5	5	–1.6	–1.6	
	4.6	5	–0.4	–0.4	
	9.5	10	–1	–	
Dynamic, C_L = 50 pF					
Status Flag Disconnect to- STATUS OUT Delay, t_{ss}	–	5	200	200	ns
	–	10	100	–	
Receiver Register Disconnect to- DATA OUT Delay, t_{RDB}	–	5	200	200	ns
	–	10	100	–	
Total Power Dissipation, P_D at 3.2 MHz	–	5	5	7	mW
	–	10	15	–	

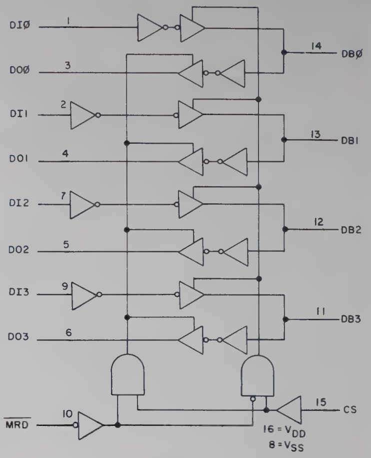
UART (Mode 0)
CDP1854



UART (Mode 1)
CDP1854



4-Bit Bus Buffer/Separator
CDP1857 (I/O)



- Allows simple expansion of I/O
- Connects directly to CPU's bidirectional data bus
- Non-inverting fully buffered data transfer
- Compatible with CDP1802 microprocessor at maximum speed
- CHIP SELECT input for simple system configurations
- Low quiescent and operating power

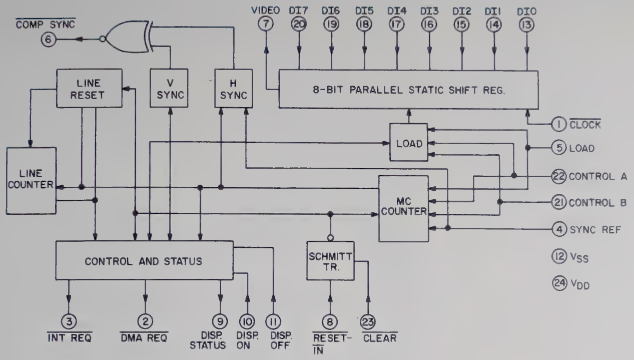
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1857D		CDP1857CD		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range	–	4	12	4	6	V
Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES AT $T_A = 25^\circ C$		UNITS
		V_O (V)	V_{DD} (V)	CDP1857D	CDP1857CD	
Static						
Quiescent Device Current, I_L Max.		– – –	5 10 15	50 100 500	100 – –	µA
Output Low (Sink) Current, I_{OL} Min.	Any Output	0.4 0.5	5 10	1.6 3.6	1.6 –	mA
Output High (Source) Current, I_{OH} Min.	Any Output	4.6 9.5	5 10	–1.6 –3.6	–1.6 –	
Dynamic: t_r, t_f = 10 ns, C_L = 100 pF						
Propagation Delay Time: $\overline{\text{MRD}}$ or CS to DO,, t_{ED}		– –	5 10	150 75	150 –	ns
$\overline{\text{MRD}}$ or CS to DB, t_{EB}		– –	5 10	150 75	150 –	ns
DI to DB, t_{IB}		– –	5 10	100 50	100 –	ns
DB to DO, t_{BD}		– –	5 10	100 50	100 –	ns

Video Display Controller
CDP1861



- Interfaces directly with CDP1802 microprocessor
- Supports bit-mapped video display for graphic flexibility
- Generates composite horizontal and vertical sync
- Programmable vertical resolution for matrix display of up to 64 x 128 segments
- Real-time interrupt generator
- Clear input
- External display control
- Designed to NTSC standards

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	4 - 6	V
Input Voltage Range	–	$V_{SS} - V_{DD}$	V
Clock Input Frequency, f_{CL}	5	0 - 2.5	MHz

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS		TYPICAL VALUES AT T_A = 25°C	UNITS
		V_O (V)	V_{DD} (V)		
Quiescent Device Current, I_L Max.		–	5	500	μA
Output Drive Current:					
Video or Sync	Output Low (Sink), I_{OL} Min.	0.4	5	1.2	mA
	Output High (Source), I_{OH} Min.	4.5	5	1	
Reset Out or Flag	Output Low (Sink), I_{OL} Min.	0.4	5	−0.4	mA
	Output High (Source), I_{OH} Min.	4.5	5	0.4	
I/O Requests;	Output Low (Sink), I_{OL} Min.	0.4	5	−0.2	mA
Reset-In: Positive Trigger Threshold, V_P		–	5	2.5	V
Negative Trigger Threshold, V_N		–	5	1.7	V
Hysteresis Voltage, V_H		–	5	0.8	V

Cross-Reference Guide

Note: RCA functionally equivalent type may not be identical with other manufacturer's type in every detail. Refer to published data for further information.

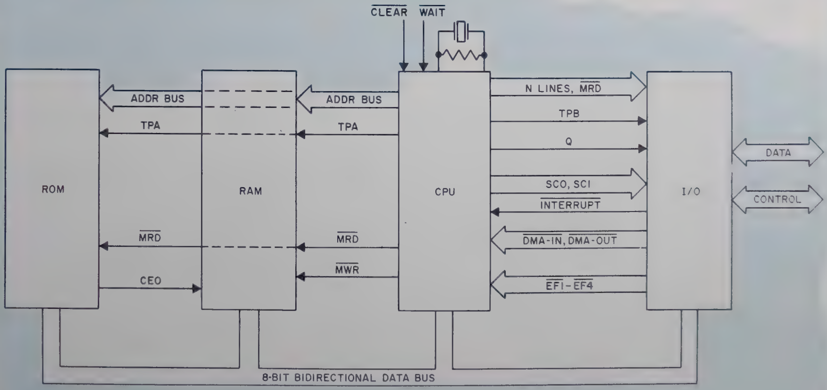
Type	Description	RCA Functionally Equivalent Type
AMI		
S4025	1024 x 1 RAM	CDP1821S
S6508	1024 x 1 RAM	CDP1821S
S5101	256 x 4 RAM	CDP1822S*
S6810-1	128 x 8 RAM	CDP1823S
S3514	512 x 8 ROM	CDP1831 CDP1832
S6830	1024 x 8 ROM	CDP1833 CDP1834
S1883	UART	CDP1854
Fairchild		
MK3514	512 x 8 ROM	CDP1831 CDP1832
MK386k	I/O	CDP1852
MK35342	1024 x 1 RAM	CDP1821S
MK35345	1024 x 1 RAM	CDP1821S
MK93415	1024 x 1 RAM	CDP1821S
MK93425	1024 x 1 RAM	CDP1821S
General Instruments		
RA-3-4256	256 x 4 RAM	CDP1822S
RO-3-4096	512 x 8 ROM	CDP1831 CDP1832
AY-3-1013 AY-3-1014 AY-3-1015	UART	CDP1854*
Hughes		
HMPS1802	CPU	CDP1802*
HMPS1824	32 x 8 RAM	CDP1824*
HMPS1822	256 x 4 RAM	CDP1822*
HMPS1852	I/O Port	CDP1852*
Intel		
2102	1024 x 1 RAM	CDP1821S*
2101	256 x 4 RAM	CDP1822S*
2111	256 x 4 RAM	CDP1822S
2112	256 x 4 RAM	CDP1822S
4101	256 x 4 RAM	CDP1822S
5101	256 x 4 RAM	CDP1822S
8101	256 x 4 RAM	CDP1822S
2308	1024 x 8 ROM	CDP1833 CDP1834
8308	1024 x 8 ROM	CDP1833 CDP1834
2704	512 x 8 PROM	CDP1831 CDP1832*
2708	1024 x 8 PROM	CDP1833 CDP1834
8708	1024 x 8 PROM	CDP1833 CDP1834
8212	Byte I/O	CDP1852
3212	Byte I/O	CDP1852
Intersil		
IM6508	1024 x 1 RAM	CDP1821S
IM6551	256 x 4 RAM	CDP1822S
IM6402/6403	UART	CDP1854*
Mostek		
MK4009-9	1024 x 1 RAM	CDP1821S
MK4102P-1	1024 x 1 RAM	CDP1821S*
MK4102N-1	1024 x 1 RAM	CDP1821S*
MK2500P	512 x 8 ROM	CDP1831 CDP1832
MK2600P	512 x 8 ROM	CDP1831 CDP1832
Motorola		
MCM2102	1024 x 1 RAM	CDP1821S*
MCM6810A	128 x 8 RAM	CDP1823S
MCM6830 MCM65308 MCM68308	1024 x 8 ROM	CDP1833 CDP1834
National		
INSB212	I/O	CDP1852
MM74C930	1024 x 1 RAM	CDP1821S
MM87S295/6	512 x 8 EAROM	CDP1831 CDP1832
MM2102	1024 x 1 RAM	CDP1821S*
MM5204C	512 x 8 PROM	CDP1831 CDP1832
MM5232	512 x 8 ROM	CDP1831 CDP1832
MM5233	512 x 8 ROM	CDP1831 CDP1832
Texas Instruments		
TMS4039	256 x 4 RAM	CDP1822S
TMS6011	UART	CDP1854*
SN54S/74S474	512 x 8 ROM	CDP1831 CDP1832
SN54S/74S475	512 x 8 ROM	CDP1831 CDP1832
Western Digital		
TR1602A	UART	CDP1854*

*Pin-for-pin compatible.

Complete 1800-Series microcomputer systems often use additional RCA solid state devices and other components

- COS/MOS Digital Integrated Circuits
- Linear Integrated Circuits
- Clocking
- Power Supplies

Typical CDP1802 microprocessor system



COS/MOS Integrated Circuits

Circuit	Function	Application
CD4016 CD4066	Transmission gates	Interfacing non-3-state output devices to the data bus
CD4049 CD4050 CD40109	Level shifters	Interfacing components of various voltage levels
CD4041 CD4050 CD4049 CD4502	Bus drivers	Bus driving into large loading
CD4028 CD4514 CD4515 CD4555 CD4556	Decoders	Memory address or N-bit lines
CD4056 CD4511	Display devices	Interfacing data bus to display devices
CD4520 CD4060	Timers/ counters	External time-keeping or sequence counting
CD40105	FIFO	Interfacing systems with different clock rates
CD40101	Parity generation decoder	Parity generation and detection
CD4034 CD4042 CD4076 CD4508	Data latches	Byte output devices
CD4014 CD4015 CD4017 CD4021 CD4034 CD4094 CD40104 CD40194	Shift registers	Serial I/O

Linear Integrated Circuits

Circuit	Function	Application
CD2500 CD2501 CD2502 CD2503	BCD-to-7-segment decoder-drivers	Display
CA3724 CA3725	1-A n-p-n transistor arrays	Relays, lamps, solenoid drivers
CA3081 CA3082 CA3083	100-mA n-p-n transistor arrays	Drivers, interfacing
CA3130 CA3140	BiMOS op-amps	High-Z_{IN} amplifiers and comparators, signal amplification, sensing
CA3085	Positive voltage regulator	On-board supply regulation
CA3078	Micropower op-amp	Low-voltage applications
CA3080	Variable-gain op-amp	Voltage comparator sample-and-hold, gain control, multiplex
CA3094	Programmable power switch/ amplifier	General-purpose control operations, timing
CA3098	Programmable Schmitt trigger with memory	Control applications, time delays, Schmitt trigger switching
CA3600	COS/MOS transistor array	Linear operation
CA3062	Photodetector and power amplifier	Photoelectric control
CA139 CA239 CA339	Quad voltage comparators	Multi-comparator applications
CA124 CA224 CA324	Quad op-amps	Multi-amplifier applications
CA555	Timer	Precision timing and oscillator applications

Clocking

Clock signal generation for the CDP1802 COSMAC microprocessor is simple and straightforward. The CDP1802 features of static operation and a single-phase clock make practical the use of the on-chip oscillator as the clock generator. The design of external oscillators, crystal or RC controlled, is also straightforward since they require only minimal circuitry. Recommended RC-controlled oscillator circuits include:

1. Inverter-type oscillators
2. RC oscillator using COS/MOS IC type CD4047A
3. Schmitt-trigger type RC oscillator

Any A-T cut crystal oscillator may be used as long as the crystal frequency is less than or equal to the maximum operating frequency specified in the CDP1802 data sheet. For improved stability, a parallel load capacitance of 20 to 24 pF can be used.

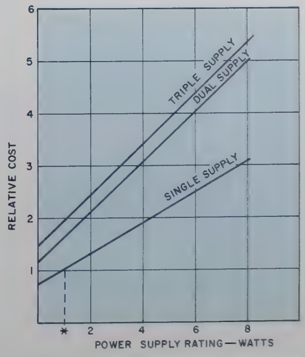
Possible crystal suppliers include:

Bliley Electronic Co.
Erie Technological Products
CTS Knights

Power Supplies

The cost of a power supply for use with CDP1800 Series microcomputer systems is minimized because of the advantages of the CMOS technology. The wide-operating-voltage range of 4 to 12 volts and the single power-supply requirement make CDP1802-based systems design simple and straightforward.

In fact, only a CMOS microprocessor like the CDP1802 is suitable for portable and battery back-up applications. Microprocessor systems incorporating the CDP1802, CDP1832, CDP1824, and CDP1852 have a typical power dissipation of only 100 mW. This small power requirement minimizes power-supply costs and helps to make COSMAC systems the first and best choice in microprocessor design.



* TYPICAL POWER SUPPLY REQUIREMENTS FOR COSMAC BASED SYSTEM.

Support Systems for the CDP1802 COSMAC microprocessor include an extensive line of hardware, software, and supplemental literature.

Features

- Full spectrum of design aids: software, hardware, support, and literature
- Low cost systems for complete system design and debugging functions
- Hardware and software application support at your fingertips
- Offers "graduated steps" to microprocessor design
- Complete series of necessary literature and application notes

CDP18S012	COSMAC Microtutor II
CDP18S005	COSMAC Development System II
CDP18S805V1	Floppy Disk System
CDP18S020	COSMAC Evaluation Kit
CDP18S021	COSMAC Microterminal
CDP18S023	Power Supply
CDP18S030	COSMAC Micromonitor
CDP18S826	Fixed Point Arithmetic Package
CDP18S91X	CSDP

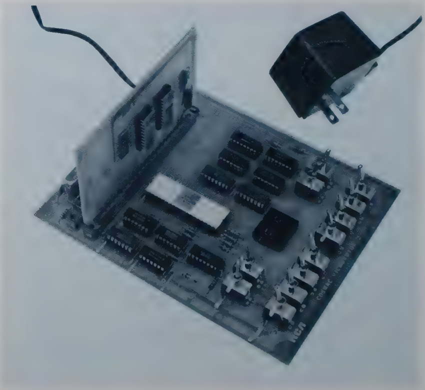
COSMAC Microtutor II

CDP18S012

To learn about programming and microprocessors

- Fully assembled unit
- Easy to use for quick hands-on microprocessor experience
- Expandable on board for additional user requirements
- Alternate data display and program instruction capability
- Complete with power supply and 256 bytes of RAM
- Dimensions:
  Base: 5" x 6.5" x 1"
  PC card: 3" x 4.5"

- Manual: MPM-209



COSMAC Development System II
CDP18S005

For complete hardware and software system development

- Resident assembler and editor included for programming ease
- Fully assembled development system
- Terminal interface connections for 20 mA loop, RS232C, and Microterminal
- Accessable, socketed CDP1802 for simple interfacing to Micromonitor (CDP18S030)
- Interfaces directly to Floppy Disk System (CDP18S805)
- 4K-byte RAM included (expandable)
- Plug-in sockets for I/O expansion
- Plug-in sockets for memory expansion
- Over-all Dimensions: Length: 19″
  Width: 11″
  Height: 6″

- Manual: MPM-216

Floppy Disk System
CDP18S805V1

For high-speed program and data processing

- Interfaces directly to COSMAC Development System (CDP18S005)
- Dual disk drive mechanism
- Monitor and disk control programs in firmware
- Programmed system diskette and blank diskette supplied
- 250K byte capability per diskette
- Rapid assembly, edit, and debug capability
- Disk-to-tape, disk diagnotic, memory save, assemblers and editor software supplied
- Additional software available
- Extra blank diskettes available (CDP18S829)
- Over-all Dimensions: Length: 20¾″
  Width: 19¼″
  Height: 7¼″

- Manual: MPM-217

Note: Alternate model with worldwide power supply also available: CDP18S805V2

COSMAC Micromonitor

CDP18S030

For in-circuit real-time hardware and software debugging.

- Stand-alone unit
- Single connection to any CDP1802 system
- 45 separate debug commands
- For field servicing, production testing, or debugging prototypes
- Minimal effects on system under test—actually uses the system's processor instead of "emulating" it
- Operates from built-in keyboard and display or interfaces external terminal for hard copy—20 mA, RS232C; 110, 300, and 1200 baud
- Data-logs several CPU registers at user determined points
- Self-contained, portable unit weighs only 16 lbs
- Built-in tracking power supply

- Over-all dimensions: Length: 18½″
  Width: 14½″
  Height: 6″

- Manual: MPM-218

COSMAC Software Development Package (CSDP)

For non-resident program development

CDP18S910V1	Magnetic Tape	32-bit version IBM-370, TSO optimized
CDP18S911V1	Card Deck	
CDP18S910V2	Magnetic Tape	32-bit version IBM-370, CMS optimized
CDP18S911V2	Card Deck	
CDP18S912	Magnetic Tape	16-bit version (HP-2100)
CDP18S913	Card Deck	
CDP18S914	Magnetic Tape	16-bit version (PDP-11)
CDP18S915	Card Deck	
CDP18S916	Magnetic Tape	32-bit version (PDP-10)
CDP18S917	Card Deck	
CDP18S918	Magnetic Tape	32-bit version (NOVA-13)
CDP18S919	Card Deck	

- Cross-assembler, simulator, and debugger
- Written in portable Fortran IV
- One-pass assembler with classical and extended assembly language power
- Versatile, powerful, and easy to use commands
- Interactive simulator/debugger acts as a "software oscilloscope" for multiple debug features
- Directly downloads programs into COSMAC Development System
- Available on timesharing networks

- Manuals: MPM-202 and MPM-204

Binary Arithmetic Subroutine

To ease programming of often used routines

CDP18S826	Diskette
CDP18S826V1	Paper Tape
CDP18S826V2	Cassette Tape

- Consists of 31 routines including register save and mathematical companion operations
- 16-bit 2's-complement arithmetic subroutines
- Easily used multiply and divide routines
- Features double precision capability for the basic functions of (+), (–), (×), and (÷)
- BCD ⇋ binary conversion

- Manual: MPM-206

Accessories

To complement your COSMAC microprocessor system development tools

For CDP18S005 (CDS II)

CDP18S102†	CDP1802 CPU Card
CDP18S103†	Control Card
CDP18S205†	4K RAM Card
CDP18S206†	Address Latch and Bank Select Card
CDP18S401†	ROM/RAM Card
CDP18S502	Extender Card
CDP18S507†	Terminal Interface Card
CDP18S508	UART Interface Card
CDP18S509†	I/O Decode Card
CDP18S510	Byte I/O Card
CDP18S801V1	Floppy Disk Drive
**CDP18S813	CDS II–Disk Interface Card
**CDP18S825	System Software (Disk)
CDP18S829	Blank Diskette

†Included with CDP18S005 (CDS II)

**Includes complete CDS-Floppy interface.

Manuals

MPM-200	COSMAC Microprocessor Library (2 vol.)
MPM-209	COSMAC Microtutor II Manual
MPM-201	User Manual for the CDP1802 COSMAC Microprocessor
MPM-202	Timesharing Manual for the CDP1802 COSMAC Microprocessor
MPM-203	Evaluation Kit Manual for the RCA-CDP1802 Microprocessor
MPM-204	Installation Manual for the RCA COSMAC Software Development Package
MPM-206	Binary Arithmetic Subroutines for RCA COSMAC Microprocessors
MPM-208	Operator Manual for the RCA COSMAC Development System (for CDP18S004)
MPM-211	Instruction Manual for the COSMAC Floppy Disk System (for CDP18S004)
MPM-212	Instruction Manual for the RCA COSMAC Microterminal
MPM-216	Operator Manual for the RCA COSMAC Development System II (CD18S005)
MPM-217	COSMAC Floppy Disk System II CDP18S005 Instruction Manual

Application Notes

General:

ICAN-6525	Guide to Better Handling and Operation of CMOS Integrated Circuits
ICAN-6562	Register-Based Output Function for RCA COSMAC Microprocessors
ICAN-6565	Design of Clock Generators for use with RCA COSMAC Microprocessors
ICAN-6581	Power-On Reset/Run Circuits for the RCA CDP1802 COSMAC Microprocessor

For use with CDS (CDP18S004):

ICAN-6482	Programmable Interval Timer and Counter for use with the RCA COSMAC Development Systems
ICAN-6485	Interrupt Priority Resolution Circuit for use with RCA COSMAC Development Systems
ICAN-6486	Adding Two-Level I/O Interface Capability to RCA COSMAC Development Systems
ICAN-6487	Hexadecimal Display for use with RCA COSMAC Development Systems
ICAN-6488	Alphanumeric Display for use with RCA COSMAC Development Systems
ICAN-6490	Analog-to-Digital Converter for use with RCA COSMAC Development Systems
ICAN-6491	PROM Programmer for RCA COSMAC Development Systems
ICAN-6516	Hexadecimal Keyboard Interface for use in the RCA COSMAC Development Systems

COSMAC Register and Instruction Summary

Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer
N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high-order 4 bits)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip-Flop

Instruction Set

The COSMAC instruction summary is given below. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P
R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation
M(R(N)) → D; R(N) + 1

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

Instruction Summary

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D; R(N) +1
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X) +1
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P) +1
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X) –1
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) +1
DECREMENT REG N	DEC	2N	R(N) –1
INCREMENT REG X	IRX	60	R(X) +1
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1
LOGIC OPERATIONS♦♦			
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P) +1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P) +1
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P) +1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76♦	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E♦	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL		

Instruction Summary (cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS♦♦			
ADD	ADD	F4	M(R(X)) +D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) +D→DF, D; R(P) +1
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) +D +DF→DF, D R(P) +1
SUBTRACT D	SD	F5	M(R(X))–D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))–D→DF, D; R(P) +1
SUBTRACT D WITH BORROW	SDB	75	M(R(X))–D–(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))–D–(NOT DF)→DF, D; R(P) +1
SUBTRACT MEMORY	SM	F7	D–M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D–M(R(P))→DF, D; R(P) +1
SUBTRACT MEMORY WITH BORROW	SMB	77	D–M(R(X))–(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D–M(R(P))–(NOT DF)→DF, D R(P) +1
BRANCH INSTRUCTIONS–SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38♦	R(P) +1
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF DF=1	BDF	33♦	IF DF=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B♦	IF DF=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=1	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=0	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=1	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=0	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=1	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=0	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=1	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=0	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P) +1
BRANCH INSTRUCTIONS–LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P) +1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8♦	R(P) +2
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2

Instruction Summary (cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38[◆]	R(P) +1
LONG SKIP (SEE NLBR)	LSKP	C8[◆]	R(P) +2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2 ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00[#]	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)–1
RETURN	RET	70	M(R(X))→(X,P); R(X) +1 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X) +1 0→IE
INPUT–OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) +1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) +1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) +1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) +1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) +1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) +1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) +1; N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7

[◆] THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

[◆◆] THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.
AFTER AN ADD INSTRUCTION:
DF = 1 DENOTES A CARRY HAS OCCURRED
DF = 0 DENOTES A CARRY HAS NOT OCCURRED
AFTER A SUBTRACT INSTRUCTION:
DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
THE SYNTAX–(NOT DF) DENOTES THE SUBTRACTION OF THE BORROW

[#] An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch.

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.
   The short-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test the status (1 or 0) of the four EF flags
   f) Effect an unconditional no branch
   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch with the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch.

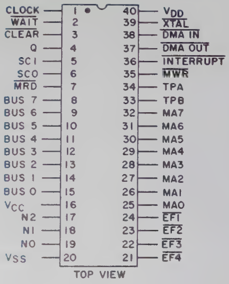
3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

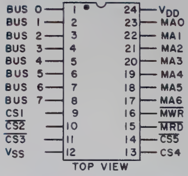
   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).
   They can:
   a) Skip unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test for IE=1
   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

Terminal Assignment Diagrams

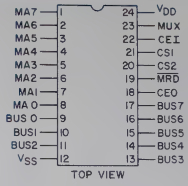
CDP1802
COSMAC
Microprocessor



CDP1823S
128 x 8 RAM



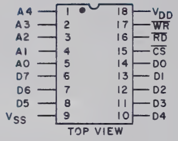
CDP1833
1024 x 8 ROM



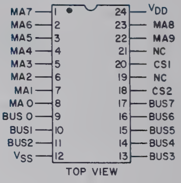
NC = NO CONNECTION

92CS-28889

CDP1824
32 x 8 RAM

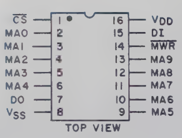


CDP1834
1024 x 8 ROM

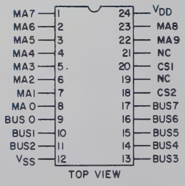


NC = NO CONNECTION

CDP1821S
1024 x 1 RAM

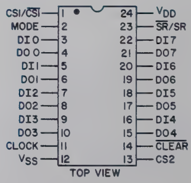


CDP1831
512 x 8 ROM

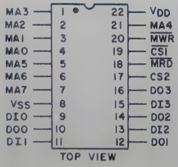


NC = NO CONNECTION

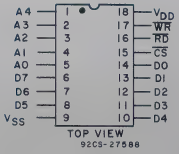
CDP1852
Byte I/O



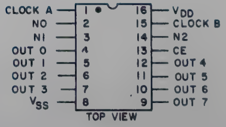
CDP1822S
256 x 4 RAM



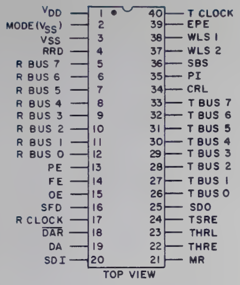
CDP1832
512 x 8 ROM



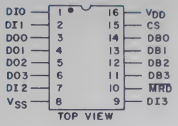
CDP1853
N-Bit Decoder



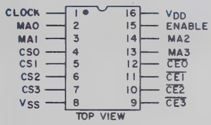
CDP1854 UART Mode 0



CDP1856, CDP1857 Bus Buffers

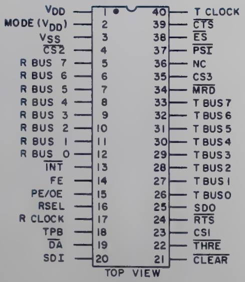


CDP1858 4-Bit Latch



CLOCK 1 16 V_{DD}
MA0 2 15 ENABLE
MA1 3 14 MA2
CS0 4 13 MA3
CS1 5 12 $\overline{CE0}$
CS2 6 11 $\overline{CE1}$
CS3 7 10 $\overline{CE2}$
V_{SS} 8 9 $\overline{CE3}$
TOP VIEW

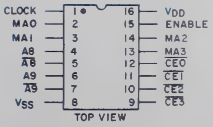
CDP1854 UART Mode 1



V_{DD} 1 40 T CLOCK
MODE (V_{DD}) 2 39 $\overline{CTS}$
V_{SS} 3 38 $\overline{ES}$
$\overline{CS2}$ 4 37 $\overline{PSI}$
R BUS 7 5 36 NC
R BUS 6 6 35 CS3
R BUS 5 7 34 $\overline{MRD}$
R BUS 4 8 33 T BUS 7
R BUS 3 9 32 T BUS 6
R BUS 2 10 31 T BUS 5
R BUS 1 11 30 T BUS 4
R BUS 0 12 29 T BUS 3
$\overline{INT}$ 13 28 T BUS 2
FE 14 27 T BUS 1
PE/OE 15 26 T BUS 0
RSEL 16 25 SDO
R CLOCK 17 24 $\overline{RTS}$
TPB 18 23 CS1
$\overline{DA}$ 19 22 $\overline{THRE}$
SDI 20 21 $\overline{CLEAR}$
TOP VIEW

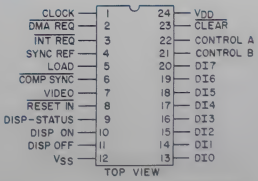
NC=NO CONNECTION

CDP1859 4-Bit Latch



CLOCK 1 16 V_{DD}
MA0 2 15 ENABLE
MA1 3 14 MA2
A8 4 13 MA3
$\overline{A8}$ 5 12 $\overline{CE0}$
A9 6 11 $\overline{CE1}$
$\overline{A9}$ 7 10 $\overline{CE2}$
V_{SS} 8 9 $\overline{CE3}$
TOP VIEW

CDP1861 Video Display Controller



92CS-29730

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	Spoerle Electronic KG, Otto-Hahn-Strasse 16, 6072 Dreieich	06103/604-1
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Holland	Inelco Nederland b.v., Joan Muyskenweg 22, Amsterdam 1006	(020)93 48 24
Hong Kong	Gibb, Livingston and Co., PO Box 55	
India	Comel, Sandhurst Bridge, 532 Sardar VP Road, Bombay 7 WB	
Indonesia	NVPD Soedarpo Corp., Jalan Veteran Satu 21-22, Jakarta 1/4	
Israel	Eastronics Limited, 11 Rozanis St., Tel-Baruch, PO Box 39300, Tel Aviv 61390	03 475151
Italy	Lasi Elettronica S.p.A., V. Le Lombardia 6, 20092 Cinisello Balsano, Milan	92 73 578
	Silverstar Limited, 20 Via dei Gracchi, 20146 Milan	4996
Japan	Okura Trading Co., Ltd., 3-6 Ginza Nichome, Tokyo 104	
Korea	Panwest Co., Ltd.,CPO Box 3358/903-904 Sambo Bldg., Sokong-Dong, Choong-Ku, Seoul	
Malaysia	Edward Eu & Co. (Pte) Ltd., 193, Jalan IMBI Road, Kuala Lumpur 06-23	
Mexico	Deksa, S.A.,Avenida Nuevo Leon #159, Mexico 11, D.F.	
	Mexicana de Bulbos, S.A.,Michoacan No. 30, Mexico 11,D.F.	
	Proveedora Electronica Industrial, S.A., Apartado Postal 27-599, Mexico 11, D.F.	
New Zealand	AWA New Zealand Ltd., 36-44 Adelaide Rd., PO Box 830, Wellington 2	
Norway	EGA A/S, Hjalmar Brantingsvei 6, Oslo 5	22 19 00
Paraguay	Comp. Com. del Paraguay, S.A., Casilla de Correo 344, Asuncion	
Peru	Arven S.A., Av. Jose Pardo 741, B. Miraflores, Lima 18	
Philippines	Philippine Electronic Ind., PO Box 498, Makati, Rizal D-708	
Portugal	Telectra SARL, 103 Rua Rodrigo da Fonseca, Lisbon 1	68 60 72/75
Singapore	Edward Eu and Co., No. 1 Orchard Rd., 9	
South Africa	Allied Electric S.A. (Pty) Ltd., Box 6090, Dunswart 1508	52-8232
Spain	Ataio Ingenieros SA, Enrique Laretta 10 & 12, Madrid 16	733 05 62 215 35 43
Sri Lanka	C.W. Mackie & Co., Ltd., 36 D.R. Wijewardena Mawatha, Colombo 10	
Sweden	Ferner Electronics AB, Snoermakarvaegen 35, PO Box 125, S-16126, Bromma-Stockholm	08/80 25 40
Switzerland	Baerlocher AG, PO Box 485, 8021 Zurich	01/42 99 00
Taiwan	Hwa Sheng Electr. Co., 5/F Pong Lai Bldg., 245 Min Chun East Road, Taipei	
Thailand	Anglo-Thai Eng. Ltd., PO Box 18, Bangkok	
Uruguay	American Products S.A., Av. Italia 4230, Montevideo	
Venezuela	Telereca, C.A., PO Box 3975, Caracas	
Yugoslavia	Avtotehna, PO Box 5930XI, Titova 36, Ljubjana 61000	317 044
UK	Apex Components Ltd., 396 Bath Road, Slough, Bucks, SL16 6JD	Burnham 63741
	Crellon Ltd., 380/386 Bath Road, Slough, Bucks, SL16 6JE	Burnham 4434
	REL Equipment & Components Ltd., Croft House, Bancroft, Hitchin, Herts, SG5 1BU	57181
	Semicomps (Northern) Ltd., East Bowmont Street, Kelso, Roxburghshire TD5 711N	Kelso 2366
	ITT, Edinburgh Way, Harlow, Essex, CM29 2DF	Harlow 26811
	Mogul Electronics Ltd., 273 High Street, Epping, Essex, CM 16 4DA	Epping (0378)77366

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Alabama	Hamilton-Avnet Electronics, 805 Oster Drive N.W., Huntsville, AL 35805	(205)533-1170
Arizona	Hamilton-Avnet Electronics, 2615 South 21st Street, Phoenix, AZ 85040	(602)275-7851
	Kierulff Electronics, Inc., 4134 East Wood Street, Phoenix, AZ 85040	(602)243-4101
	Liberty Electronics/Arizona, 3130 North 27th Avenue, Phoenix, AZ 85017	(602)-257-1272
California	Cramer/Los Angeles, 17201 Daimler Street, Irvine, CA 92705	(714)979-3000
	Cramer/San Francisco, 720 Palomer Avenue, Sunnyvale, CA 94086	(408)739-3011
	Electronic Supply Corp., 2486 Third Street, Riverside, CA 92507	(714)683-7300
	Elmar Electronics, Inc., 2288 Charleston Road, Mt. View, CA 94042	(415)961-3611
	Hamilton-Avnet Electronics, 575 Middlefield Road, Mt. View, CA 94042	(415)961-7000
	Hamilton-Avnet Electronics, 8917 Complex Drive, San Diego, CA 92123	(714)279-2421
	Hamilton Electro Sales, 10912 W. Washington Blvd., Culver City, CA 90230	(213)558-2020

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	Liberty/San Diego, 8248 Mercury Court, San Diego, CA 92111	**(714)565-9171**
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	Hamilton-Avnet Electronics, 5921 North Broadway, Denver, CO 80261	**(303)534-1212**
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	Schweber Electronics Corp., Finance Drive, Commerce Industrial Park, Danbury, CT 06810	**(203)792-3500**
[illegible]	**Arrow Electronics, Inc.,** 1001 NW 62nd St., Suite 402, Ft. Lauderdale, FL 33309	**(305)776-7790**
Florida	**Cramer/Hollywood,** 4035 North 29th Avenue, Hollywood, FL 33022	**(305)945-4176**
	Cramer/Orlando, 345 Graham Avenue, Orlando, FL 32803	**(305)894-1511**
	Hamilton-Avnet Electronics, 6800 N.W. 20th Avenue, Ft. Lauderdale, FL 33309	**(305)971-2900**
	Schweber Electronics Corp., 2830 North 28th Terrace, Hollywood, FL 33020	**(305)927-0511**
Georgia	**Arrow Electronics, Inc.,** 3406 Oak Cliff Rd., Doraville, GA 30340	**(404)455-4054**
	Cramer/Atlanta, 6456 Warren Drive, Norcross, GA 30071	**(404)448-9050**
	Hamilton-Avnet Electronics, 6700 185 Access Road, Suite 1E, Norcross, GA 30071	**(404)448-0800**
Illinois	**Cramer/Chicago,** 1911 South Busse Road, Mt. Prospect, IL 60056	**(312)593-8230**
	Hamilton-Avnet Electronics, 3901 North 25th Avenue, Schiller Park, IL 60176	**(312)678-6310**
	Newark Electronics, 500 North Pulaski Road, Chicago, IL 60624	**(312)638-4411**
	Schweber Electronics Corp., 1275 Brummel Ave., Elk Grove Village, IL 60007	**(312)593-2740**
	Semiconductor Specialists, Inc., 195 Spangler Avenue, Elmhurst, IL 60126	**(312)279-1000**
Indiana	**Graham Electronics Supply, Inc.,** 133 S. Pennsylvania Street, Indianapolis, IN 46204	**(317)634-8202**
Iowa	**Deeco, Inc.,** 2500 16th Avenue, S.W., Cedar Rapids, IA 52801	**(319)365-7551**
Kansas	**Hamilton-Avnet Electronics,** 37 Lenexa Industrial Center, Lenexa, KS 66215	**(913)888-8900**
	Radio Supply Company, 115 Laura, Wichita KS 67211	**(316)267-5214**
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	Cramer/Washington 16021 Industrial Drive, Gaithersburg, MD 20760	**(301)948-0110**
	Hamilton-Avnet Electronics, 7255 Standard Drive, Hanover, MD 21076	**(301)796-5000**
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	Schweber Electronics Corp., 213 Third Avenue Waltham, MA 02154	**(617)890-8484**
	Sterling Electronics, Inc., 411 Waverly Oak Road, Waltham, MA 02154	**(617)926-9720**
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	RS Electronics, Inc., 3444 Schoolcraft, Livonia, MI 48150	**(313)525-1155**
	Schweber Electronics Corp., 86 Executive Drive, Troy, MI 48084	**(313)583-9242**
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Cramer/Rochester,
3000 South Winton Road,
Rochester, NY 14623 .... **(716)275-0300**
Cramer/Syracuse,
6716 Joy Road,
Syracuse, NY 13057 .... **(315)437-6671**
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167 Clay Road,
Rochester, NY 14623 .... **(716)442-7820**
Hamilton-Avnet Electronics,
6500 Joy Road,
East Syracuse, NY 13057 .... **(315)437-2641**
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Rochester, NY 14623 .... **(716)461-4000**
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Dallas, TX 75240 .... **(214)661-8661**
Hamilton-Avnet Electronics,
3939 Ann Arbor Street,
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14177 Proton Road,
Dallas, TX 75240 .... **(214)661-5010**
Schweber Electronics Corp.,
7420 Harwin Drive,
Houston, TX 77036.................... **(713)784-3600**
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Austin, TX 78758 .... **(512)836-1341**
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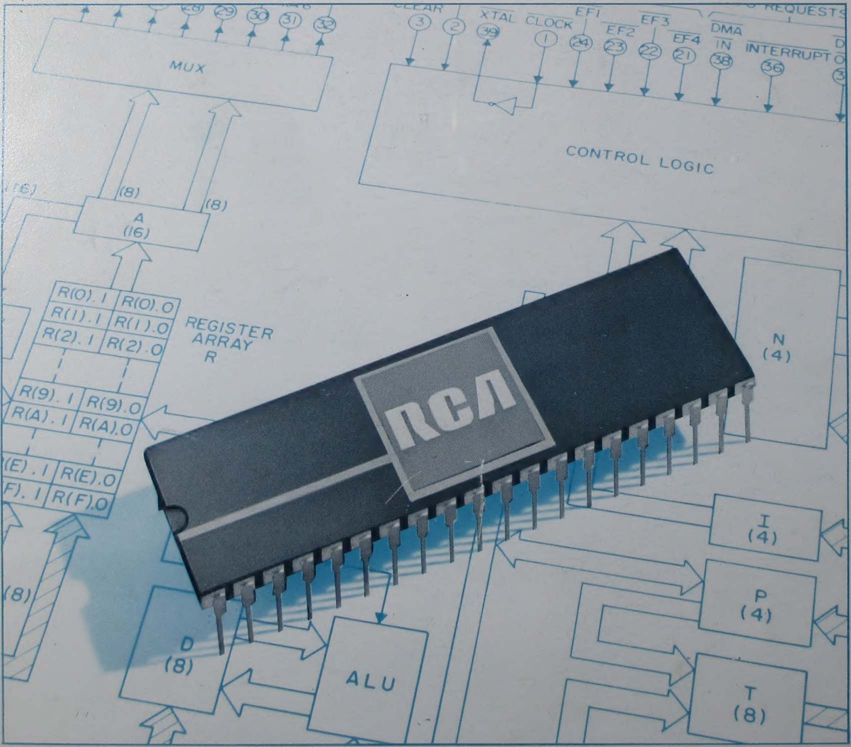
RCA Solid State



COSMAC Evaluation Kit
CDP18S020

Complete system for machine-language programming and prototyping

- Prototyping and evaluation system for the COSMAC family
- Serial interfacing capability to 20 mA loop or RS232 terminals
- Microterminal option available (CDP18S021)
- 256 bytes of RAM included
- Memory expandable on-board to 4K (pre-bussed)
- Large separate area for user circuitry
- Single-step capability
- On-board monitoring capability
- Memory Address, Data, State Code, Q-Line, Clear, Wait signals all monitored and displayed on LEDs

- Over-all Dimensions: 14″ x 9.7″
  User I/O Area: 7″ x 4″

- Manuals: MPM-203 and MPM-201

COSMAC Microterminal
CDP18S021

Low-cost alternative for TTY, CRT, or other intelligent terminals

- Fully assembled, portable, self-contained terminal
- Plugs directly into Evaluation Kit and CDS
- 8-digit, 7-segment, LED hexadecimal display
- Features simultaneous memory address and data display
- Display can be used as an output under user software control

- Over-all Dimensions: Length: 5.5″
  Width: 3″
  Height: 0.7″

- Manual: MPM-212

Power Supply
CDP18S023

Lightweight, inexpensive system power supply

- Powers Evaluation Kit and Microterminal at 5V
- Plugs into any standard wall outlet
- Ratings:
  Input – 110V, 50-60 Hz, 9W
  Output – 5VDC, 600 mA

- Over-all Dimensions: Length: 3.5″
  Width: 1.75″
  Height: 2″

Assembled Evaluation Kit With Microterminal and Power Supply